UM10056

ISP1761 Hi-Speed USB controller PCI demo board

Rev. 03 — 18 March 2008 **User manual**

Document information

Info	Content
Keywords	isp1761, drd, dual-role, dual role, peripheral, host controller, usb2, universal serial bus, otg, on-the-go, otg controller
Abstract	This PCI eval board allows ISP1761 functionality to be demonstrated on an x86-based computer, with at least one PCI slot available.

Revision history

Rev	Date	Description
03	20080318	Third version. Section 4.1: updated for clarity. Fig 3: added pin sequence to J2. Section 4.3: updated. Section 6.2: updated. Fig 10: updated pin 117 termination.
02	20080111	Second revision. Replaced paragraph 1, Section 4.3. Section 3: Specified that the PC type must be x86-based, and for the Red Hat Linux kernel support, the user is to check with NXP regarding the latest driver versions supported. Corrected Fig 10. Updated the names of ISP1761 host and peripheral controller installation guides. Removed instances of ISP176x.
01	20060509	First release.

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1. Introduction

The ISP1761 is a Hi-Speed Universal Serial Bus (USB) On-The-Go (OTG) dual-role controller with three USB ports. Port 1 is configurable as a host controller or a peripheral controller, while ports 2 and 3 are always assigned to the host controller.

The ISP1761 is accessible through a generic processor interface, with demultiplexed address and data lines.

The PCI evaluation (eval) board allows demonstrating the functionality of the ISP1761 on a standard PC with at least one PCI slot.

A PLX9054 and a CPLD ensure interface from PCI-to-generic-processor interface type, which is specific to the ISP1761.

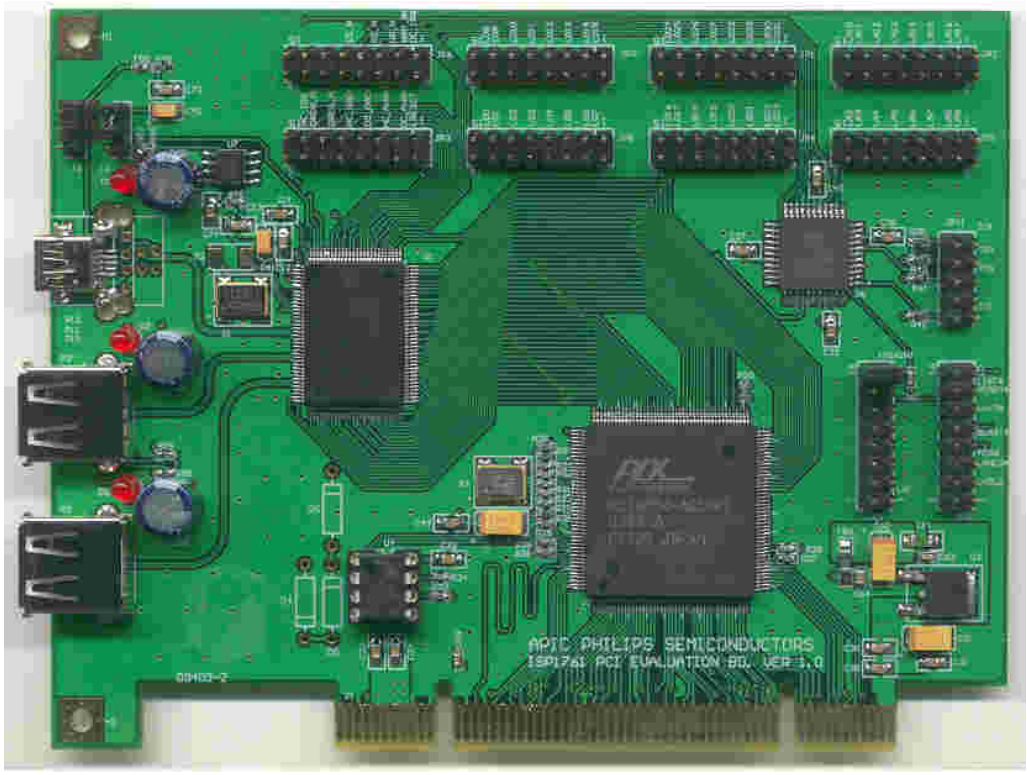

Fig 1. ISP1761 PCI eval board

2. ISP1761 PCI eval board features

- Complies with *PCI Local Bus Specification Version 2.2*
- Uses PLX9054 for PCI-to-local-bus interfacing
- Three USB ports: two are host controllers and one is configurable as host controller or peripheral controller
- 50 MHz PLX9054 local bus clock and 50 MHz CPLD clock
- Configurable ISP1761 interrupt polarity; INTA# used on the PCI
- Optional use of a 12 MHz crystal or a 12 MHz oscillator

- Optional configuration for the analog or digital overcurrent protection
- All local bus signals are easily accessible on test headers designed for direct connection of a standard Tektronix logic analyzer
- PLX9054 is configurable at start-up using a 93C56 serial EEPROM
- Flexible configuration of port 1 using Type A, Type B or OTG mini-AB connector
- Jumper J2 to configure pin ID, if a Type A or Type B connector is soldered for port 17
- Jumper J3 to configure port 1 to use the internal charge pump of the ISP1761[1] or an external power switch

3. System requirements

You can use any x86-based computer that has an available PCI slot (32 bits, 33 MHz) running Linux Red Hat kernel. For the kernel versions supported, please check with NXP for the latest driver versions available. The type of Linux Red Hat installation determines minimum system requirements. The minimum recommended system configuration is a Pentium-class processor (1 GHz) with 128 MB RAM.

4. Jumper settings

The ISP1761 PCI eval board has the following jumper settings:

4.1 JP9

Pins 15 and 16 of JP9 are used to set the interrupt polarity according to the ISP1761 IRQ polarity programming.

For ISP1761 IRQ polarity active LOW: JP9 must be on. JP9.15 and JP9.16 are shorted.

For ISP1761 IRQ polarity active HIGH: JP9 must be off. JP9.15 and JP9.16 are not shorted.

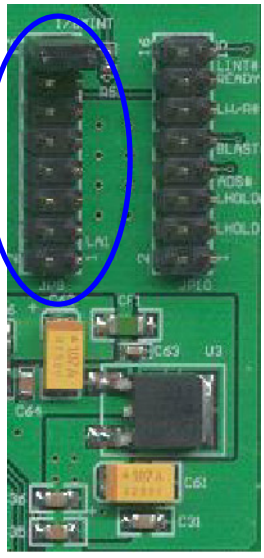

Fig 2. Jumper JP9

1. Using the OC1_N pin to generate V_{BUS} with 50 mA (maximum) when V_{CP_IN} = 3.3 V.

4.2 J2

J2 defines the logic level of the ID pin.

For the A-device: The jumper must be connected on 2 to 3 (HIGH).

For the B-device: The jumper must be connected on 1 to 2 (LOW).

J2 is used only if the USB connector for port 1 is a Type A or Type B and not the OTG connector that will automatically toggle the ID pin logic level, depending on the type of the OTG cable.

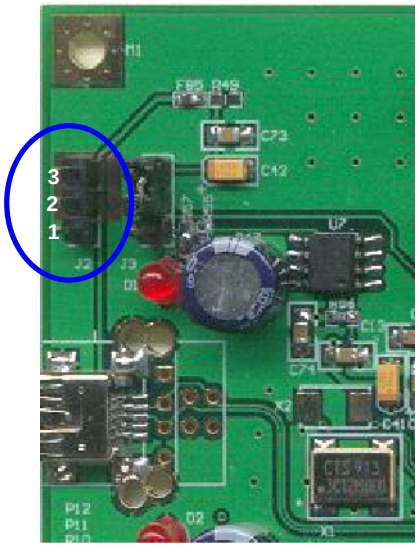

Fig 3. Jumper J2

4.3 J3

Jumper J3 can be set as follows to configure port 1 as a host or OTG:

- J3 is connected on 1 to 2: This means that port 1 is configured as a host and external power supply is used.
- J3 is connected on 2 to 3. This means that port 1 is in OTG mode and internal power supply is used.
- J3 is shorted on 1, 2 and 3. Port 1 can be configured as a host or OTG depending on the connector used. If P12 is mounted, port 1 is in OTG mode, and if P10 is mounted, port 1 is in host mode. In both the cases, external power supply is used.

Solder R57 when the ISP1761 is using the external power switch and the digital over current scheme with MIC2026. R56 must be populated only when implementing the analog overcurrent scheme.

For a better understanding of this jumper setting, see Fig 14.

The OC1_N pin will be configured for the overcurrent detection. The external power switch generates V_{BUS}.

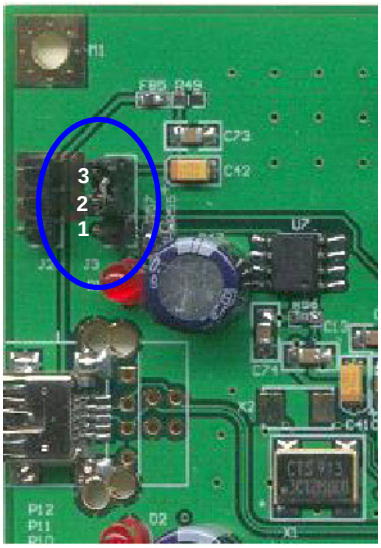

Fig 4. Jumper J3

5. Installing Linux modules

For details on installation and use of these modules, refer to *Installation Guide for the ISP1761 Peripheral Controller on Linux 2.6.9* and *Installation Guide for ISP1761 HCD on Linux 2.6.20.*

6. ISP1761 eval board schematics description

6.1 USB ports

The ISP1761 has three ports.

- Port 1 can be connected to either the host controller or the peripheral controller.
- Ports 2 and 3 are always configured as host controllers.

The default connector soldered on port 1 is a Type B USB connector because port 1 will usually be used as a peripheral. Port 1 is by default routed to the peripheral controller at start-up. It is also possible to solder a Type A or an OTG USB connector on port 1; these options are also present on the PCB.

Port 1 can be configured for OTG functionality. The host-peripheral or OTG configuration of port 1 is done by programming the OTG Control register. For details, refer to the ISP1761 data sheet.

The ID pin must be tied to GND, if port 1 is intended to be always host controller; otherwise it should be pulled up as shown in Section 7.

Programming port 1 of the ISP1761 to be used as a host controller will determine the internal peripheral block to enter suspend mode, without any additional programming. Jumper J3 configures the connection and functionality of the OC1_N/V_{BUS} pin.

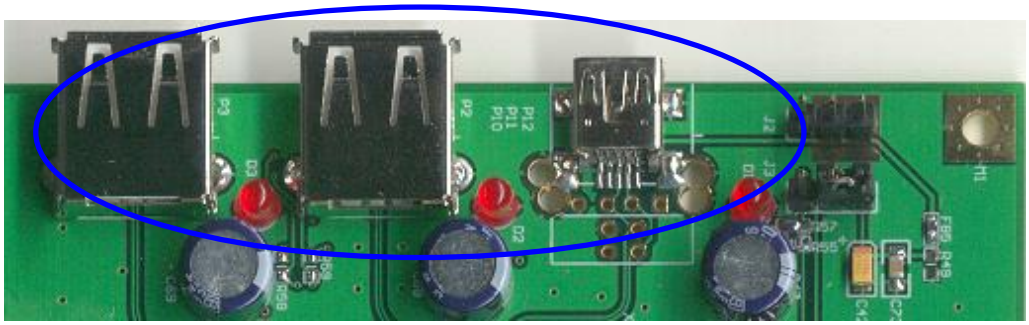

Fig 5. USB ports

6.2 LED indicators

There is a port power LED indicator for each port. Each LED will be on as soon as the port power of the respective port is enabled by software, for example, after loading the USB Host Controller Drivers (HCDs).

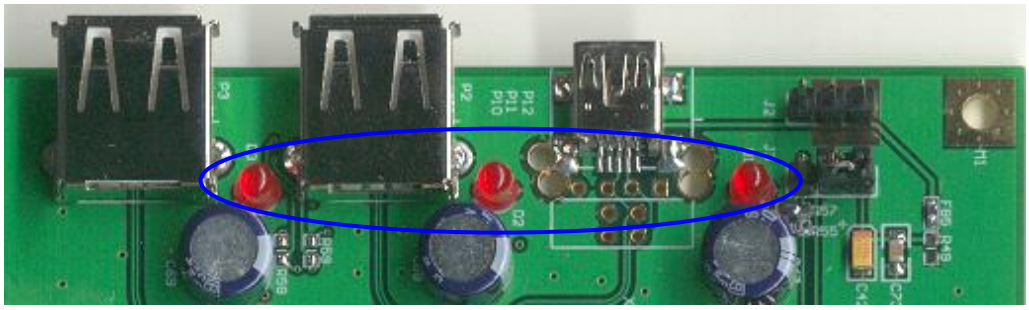

Fig 6. LED indicators

6.3 Port power switching and overcurrent detection circuit

The overcurrent detection circuit can be implemented using the digital or analog ISP1761 internal detection circuit. The ISP1761 eval board PCB is designed for both the options; either one can be optionally soldered.

6.4 Power sources and voltage regulator

A linear voltage regulator (3.3 V output) provides power for the ISP1761, PLX9054 and CPLD. The input to the regulator is PCI 5 V. The V_{BUS} voltage for USB ports is generated from the PCI 5 V source.

6.5 93C56 EEPROM

After power-on or assertion of the PCI_RESET signal, PLX9054 attempts to read the serial EEPROM to check its presence.

The 93C56 EEPROM is required for the correct initialization of PLX9054. The serial EEPROM contains information required to initialize PLX9054 registers. For details, refer to Chapter 11 of *PLX PCI 9054 Data Book*.

The initial programming of 93C56 must be done in a serial EEPROM programmer. Displaying and adjusting of certain parameters can be done using the PLXmon utility.

Fig 7. 93C56 EEPROM

6.6 PLX9054

PLX9054 is a PCI-to-local-bus accelerator. The ISP1761 is always a PCI target during initialization, as well as during the data transfer phase to or from the ISP1761 memory.

Fig 8. PLX9054

6.7 Altera EPM7064 CPLD

CPLD ensures adaptation between the ISP1761 generic processor interface and the PLX9054 local bus interface.

CPLD programming can be done in-system by using connector JP11. Table 1 shows CPLD signals connected to the PLX9054 interface.

Fig 9. Altera EPM7064 CPLD

Table 1. CPLD signals connected to the PLX9054 interface

CPLD signal	Description
LINT#	Input to PLX9054. This is an input to PLX9054. When LINT# is asserted (LOW), a PCI interrupt (INTA#) will be generated by PLX9054.
READY#	Input to PLX9054. It indicates that read data on the bus is valid or write data transfer is completed. This is generated by CPLD to achieve the targeted access time to the ISP1761.
LW/R#	Output from PLX9054. Asserted LOW for read cycles and HIGH for write cycles.
BLAST#	Output from PLX9054. This signal is driven by the current local bus master, in this case, PLX9054 to indicate the last transfer in a bus access.
ADS#	Output from PLX9054. It indicates the valid address in a new bus access. Asserted for the first clock of the bus access.
LHOLDA	Input to PLX9054. Asserted by the local bus arbiter when the bus control is granted in response to the LHOLD signal.
LHOLD	Output from PLX9054. Asserted by PLX9054 to request the use of the local bus.
LRESET#	Output from PLX9054. Local bus reset signal is driven by PLX9054. This is asserted when PLX9054 is reset using PCI_RESET. It will ensure a correct initial state for control signals connected to the ISP1761 when RESET# is asserted.

Table 2. Other CPLD signal

CPLD signal		Description
1761INT_HIGH/NLOW		Input to CPLD. This allows testing both the LOW and HIGH active polarities for the ISP1761 interrupt signal. When this signal is pulled LOW by connecting pins 15 and 16 of jumper 20, the ISP1761 interrupt must be programmed active LOW. If the ISP1761 interrupt is programmed active HIGH, pins 15 and 16 of jumper 20 must be left open. This will always generate a correct active-LOW interrupt on INTA#.

Table 3. Other signals

CPLD signal	Description
CLK sources	The ISP1761 clock source can be an external 12 MHz crystal or a 12 MHz oscillator. Both options are present on the eval board. The PLX9054 clock source is a 50 MHz oscillator used as the local bus clock. The CPLD uses the same 50 MHz clock input, and this will determine the ISP1761 control signals timing settings.
Overcurrent protection circuitry	The ISP1761 eval board implements both the digital and analog overcurrent protection circuitry that can be optionally soldered. By default, digital overcurrent protection components are mounted for all USB ports.
Test headers	Test headers allow connection of a logic analyzer on all ISP1761 CPU interface signals and main local bus signals of PLX9054.

7. Schematics

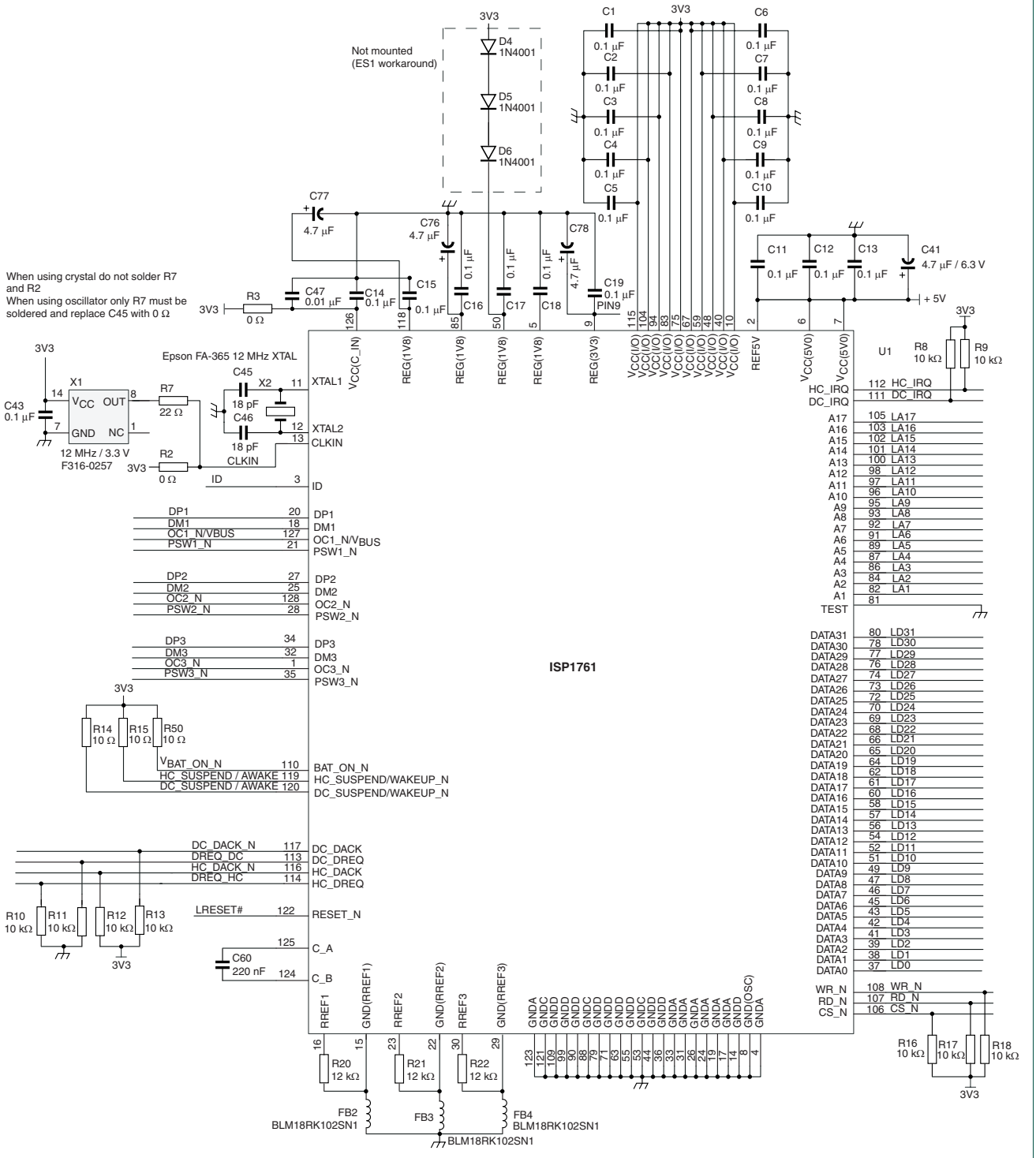

Fig 10. ISP1761

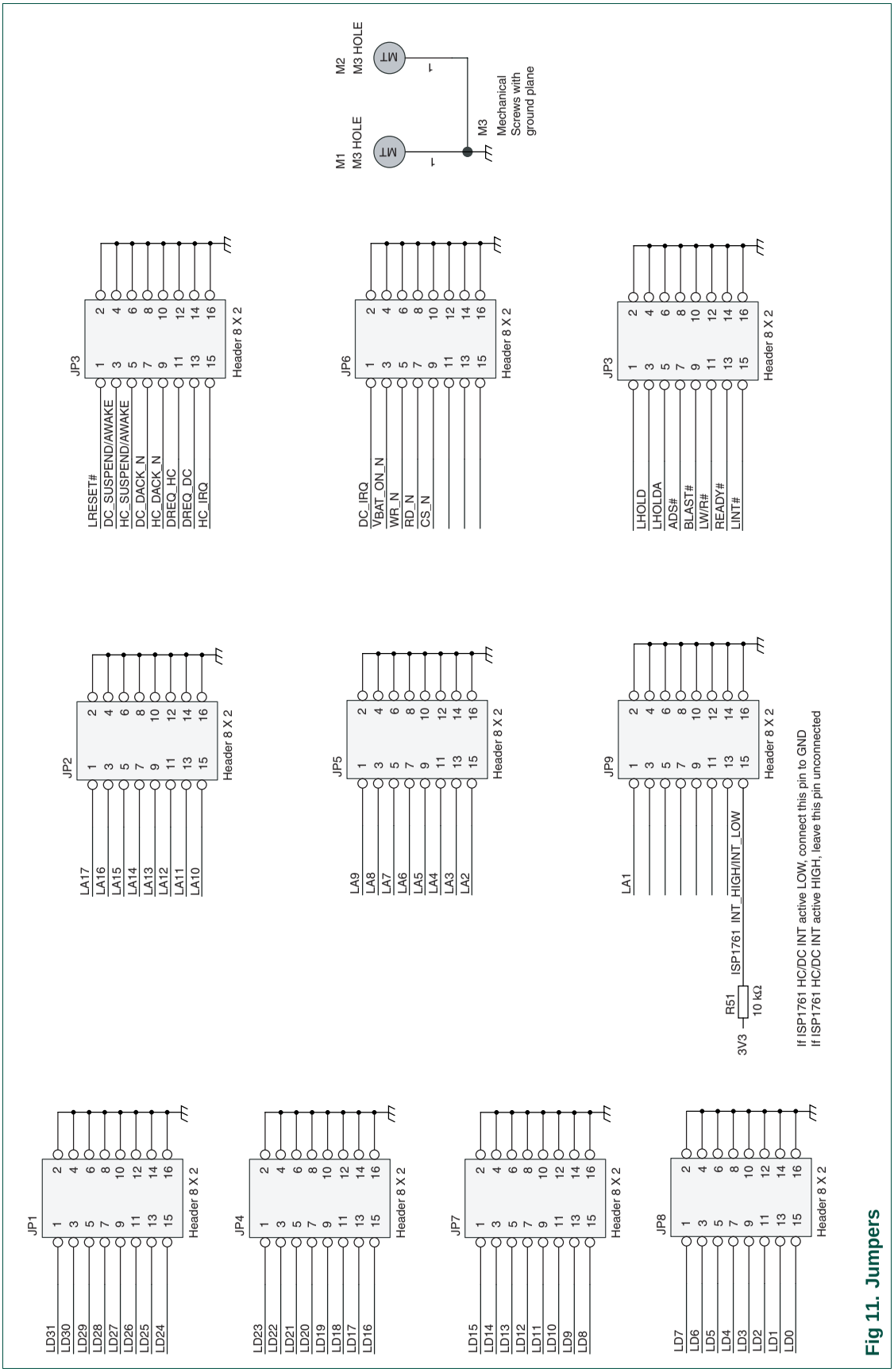

Fig 11. Jumpers

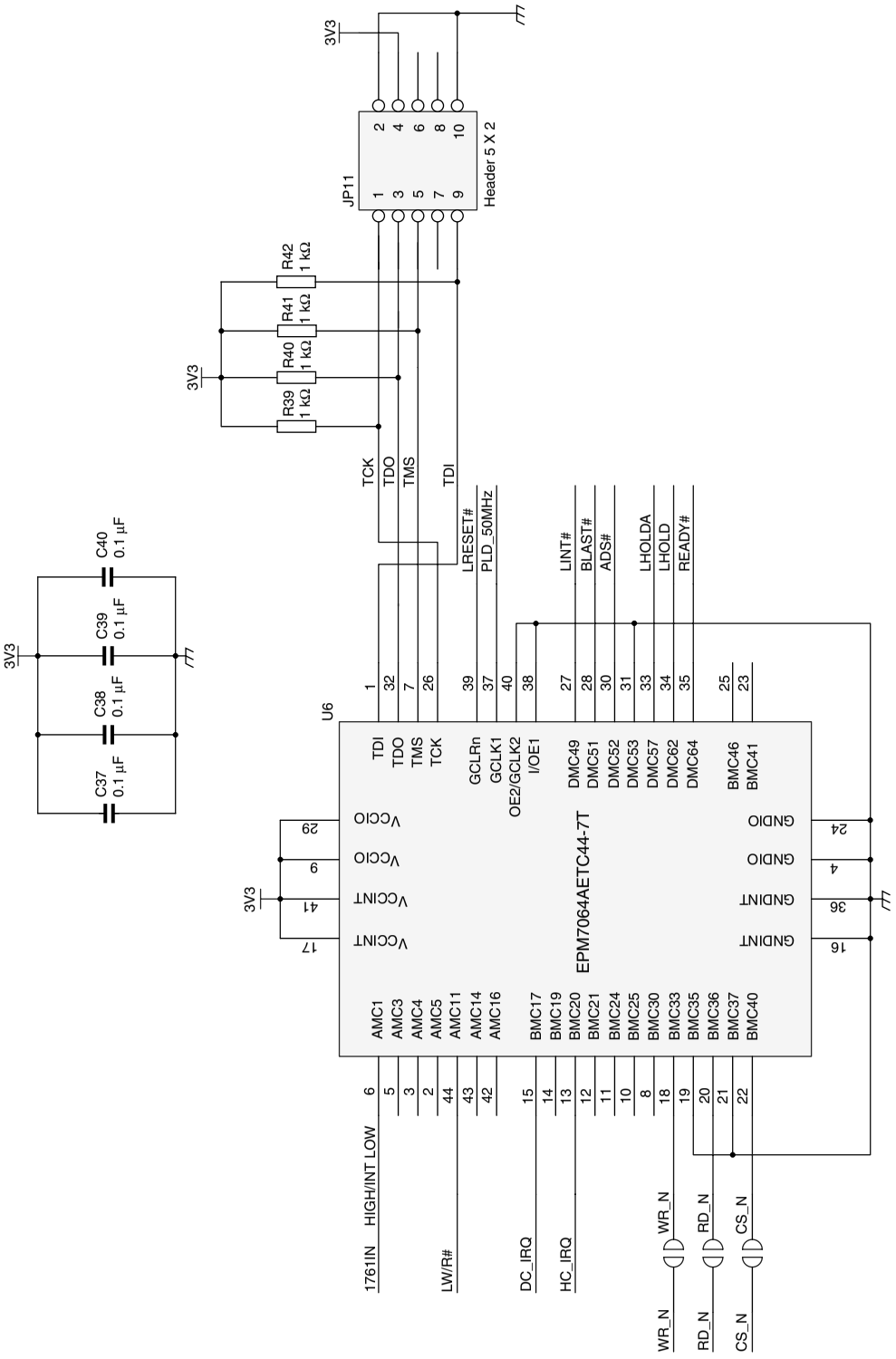

Fig 12. PLD

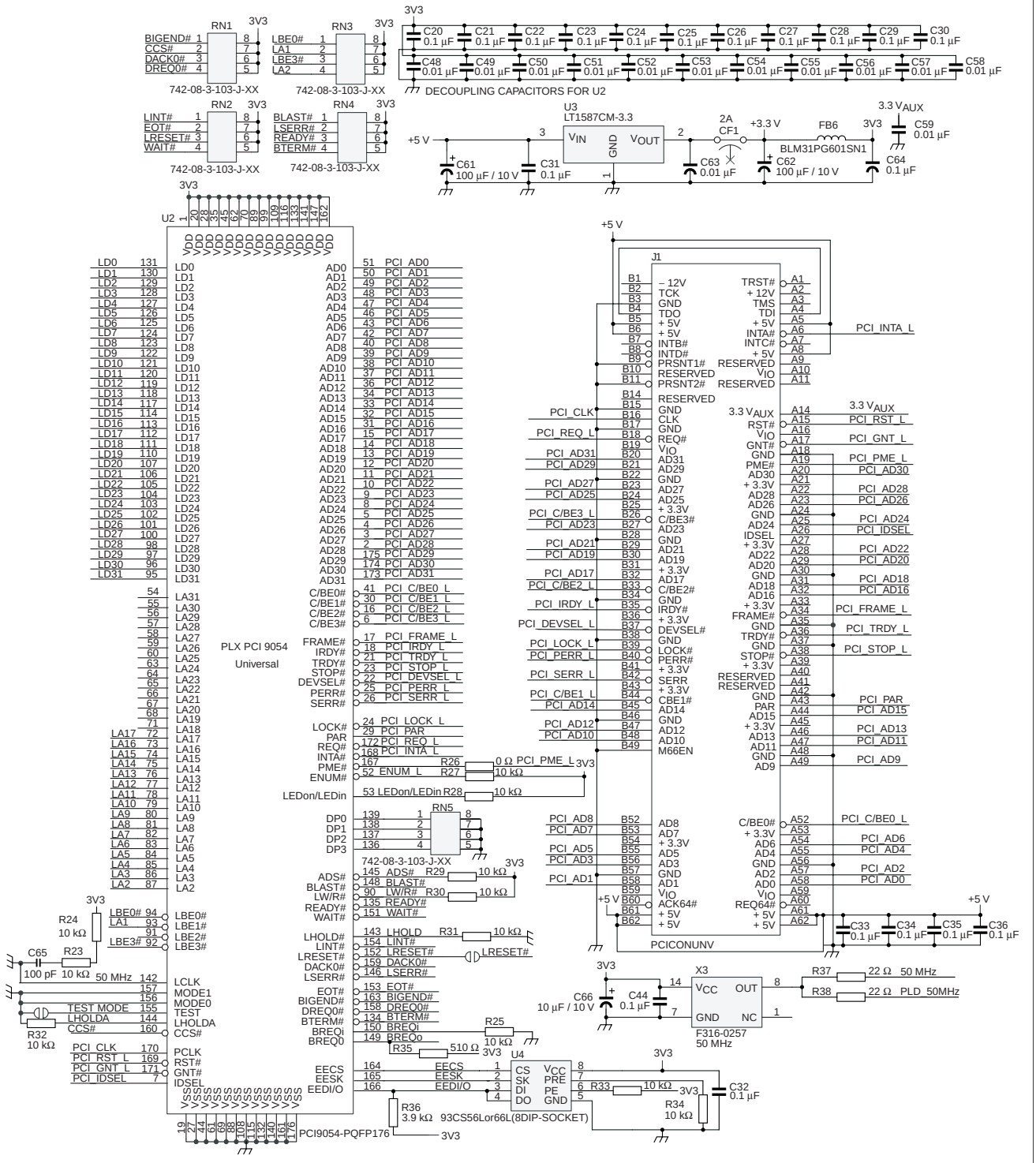

Fig 13. PCI

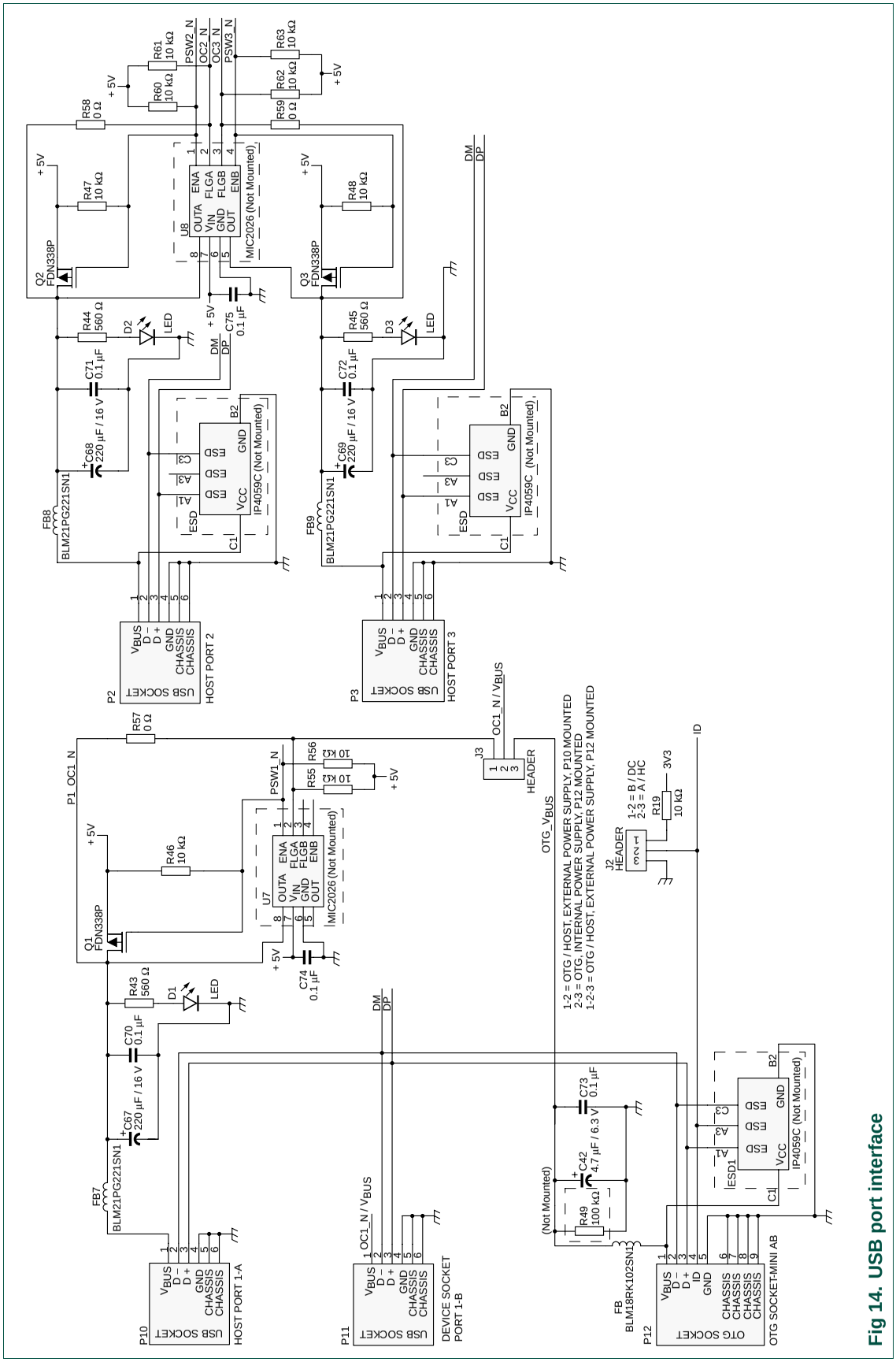

Fig 14. USB port interface

8. Bill of materials

Table 4. Bill of materials

Part Type	Designator	Footprint	Description
0.1 µF	C1, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C2, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C3, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C4, C40, C43, C44, C5, C6, C7, C70, C71, C72, C73, C74, C75, C8, C9	0805C	Capacitor
4.7 µF / 6.3 V	C41, C42	Case-A	Capacitor
18 pF	C45, C46	0603C	Capacitor
0.01 µF	C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C63	0603C	Capacitor
220 nF	C60	0603C	Capacitor
100 µF / 10 V	C61, C62	Case-C	Capacitor
0.1 µF	C64	0603C	Capacitor
100 pF	C65	0603C	Capacitor
10 µF / 10 V	C66	Case-C	Capacitor
220 µF / 16 V	C67, C68, C69	REC2/25	Capacitor
4.7 µF	C76, C77, C78	Case-A	Capacitor
2 A	CF1	1206	Fuse
LED	D1, D2, D3	LED3	LED
1N4001	D4, D5, D6	1N4001	Diode
IP4059CX5	ESD1, ESD2, ESD3	IP4059CX5	USB 2.0/USB-OTG integrated ESD protection
BLM18RK102SN1	FB2, FB3, FB4, FB5	BLM18-0603	Ferrite bead
BLM31PG601SN1	FB6	BLM31-1206	Ferrite bead
BLM21PG221SN1	FB7, FB8, FB9	BLM21-0805	Ferrite bead
PCICONUNV	J1	PCIBUS2	-
Header	J2, J3	SIP3	Header
Header 8 X 2	JP1, JP10, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9	Header 8 X 2	Header
Header 5 X 2	JP11	Header 5 X 2	Header
M3 hole	M1, M2	M_HOLE	Bracket
Host port 1-A	P10	USB-TYPEA	USB connector

Part Type	Designator	Footprint	Description
Device socket port 1-B	P11	USB-TYPEB	USB connector
OTG socket-mini AB	P12	USBII-TYPEA	Mini USB connector
Host port 2	P2	USB-TYPEA	USB connector
Host port 3	P3	USB-TYPEA	USB connector
FDN338P	Q1, Q2, Q3	FDN338P-SSOT3	P-channel 2.5 V specified power trench MOSFET
0 Ω	R2, R3	0603R	Resistor
12 kΩ	R20, R21, R22	0603R	Resistor
0 Ω	R26	0603R	Resistor SMD 1206 1/4W 2 %
10 kΩ	R27, R28, R29, R30, R31, R32, R33, R34	0603R	Resistor SMD 1206 1/4W 2 %
510 Ω	R35	0603R	Resistor SMD 1206 1/4W 2 %
3.9 kΩ	R36	0603R	Resistor
22 Ω	R37, R38	0603R	Resistor
1 kΩ	R39, R40, R41, R42	0603R	Resistor SMD 1206 1/4W 2 %
560 Ω	R43, R44, R45	0603R	Resistor 0603
10 kΩ	R46, R47, R48, R55, R56, R60, R61, R62, R63	0603R	Resistor 0603
100 kΩ	R49	0603R	Resistor 0603
0 Ω	R57, R58, R59	0603R	Resistor 0603
22 Ω	R7	0603R	Resistor
10 kΩ	R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R23, R24, R25, R4, R50, R51	0603R	Resistor
742-08-3-103-J-XX	RN1, RN2, RN3, RN4, RN5	742-08-3-103-0_8PIN_SM	Resistor
ISP1761	U1	ISP1761-LQFP128	ISP1761
PCI9054-PQFP176	U2	PQFP176-0.5	PCI bridge
LT1587CM-3.3	U3	TO-263	3A NPN LDO voltage regulator
93CS56L or 66L (8DIP-socket)	U4	NM93CS66LZ_DIP8SOCKET	EEPROM
EPM7064AETC44-7T	U6	LQFP44	CPLD
MIC2026-2	U7, U8	SO8	Current protector
12 MHz / 3.3 V	X1	XTAL-CTX	Crystal

Part Type	Designator	Footprint	Description
Epson FA-365 12 MHz XTAL	X2	XTAL-SMD5	Oscillator
50 MHz	X3	XTAL-CTX	Oscillator

9. Abbreviations

Table 5. Abbreviations

Acronym	Description
CPLD	Complex Programmable Logic Device
EEPROM	Electronically Erasable Programmable Read Only Memory
OTG	On-The-Go
PCB	Printed-Circuit Board
PCI	Peripheral Component Interconnect
USB	Universal Serial Bus

10. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] PCI Local Bus Specification Version 2.2

[3] PLX PCI 9054 Data Book

[4] Installation Guide for the ISP1761 peripheral controller on Linux 2.6.9

[5] Installation Guide for ISP1761 HCD on Linux 2.6.20

[6] ISP1761 Hi-Speed Universal Serial Bus On-The-Go controller data sheet

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